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Large-scale uniform bilayer graphene prepared by vacuum graphitization of 6H-SiC(0001) substrates

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Abstract

We report on the preparation of large-scale uniform bilayer graphenes on nominally flat Si-polar 6H-SiC(0001) substrates by flash annealing in ultrahigh vacuum. The resulting graphenes have a single thickness of one bilayer and consist of regular terraces separated by the triple SiC bilayer steps on the 6H-SiC(0001) substrates. *In situ* scanning tunneling microscopy reveals that suppression of pit formation on terraces and uniformity of SiC decomposition at step edges are the key factors to the uniform thickness. By studying the surface morphologies prepared under different annealing rates, it is found that the annealing rate is directly related to SiC decomposition, diffusion of the released Si/C atoms and strain relaxation, which together determine the final step structure and density of defects.

(Some figures may appear in colour only in the online journal)

Few-layer graphene has recently attracted much attention due to its unique physical properties and potential in future applications [1, 2]. To realize graphene-based electronics, high quality uniform graphene material over a large-scale is highly desirable. Previous studies have shown that wafer-size graphenes can be obtained by thermal decomposition of silicon carbide (SiC) [3], a well-known wide bandgap semiconductor, where Si atoms diffuse outwards from the underlying SiC substrate and desorb subsequently, and the released carbon atoms diffuse and nucleate to form graphene layers. Homogeneous monolayer graphene or graphene layers could be obtained either by annealing SiC substrates at high temperature under argon atmosphere [3, 4] or by ultrahigh vacuum (UHV) [5–7] annealing of vicinal SiC substrates. However, the high temperature annealing usually leads to step-bunching with heights of 8–15 nm [3], while high density steps on vicinal SiC substrates give rise to high electrical resistance [8], both of which degrade the device performance. Here, we present a method called flash annealing, by which we could obtain large-scale uniform bilayer graphenes over

microns with regular ordered steps of the same height. By scanning tunneling microscopy and spectroscopy (STM/STS) study of the morphology evolution under various annealing cycles and rates, the underlying mechanism for the formation of uniform bilayer graphenes is established.

The experiment was performed in a commercial Omicron UHV STM system combined with molecular beam epitaxy. The base pressure of the system is better than 2.0×10^{-10} mbar. Nominally flat nitrogen-doped 6H-SiC(0001) samples were used as substrates. After the usual degreasing process with alcohol, the samples were transferred into the UHV chamber and degassed at 650 °C for 3 h by direct current heating. The graphitization was conducted by cycles of flash annealing. The flash annealing process involves annealing of the SiC substrate from 650 to 1300 °C with a well-controlled heating rate and at 1300 °C for 30 s followed by a rapid quenching to 650 °C in 30 s. The temperature was measured with an optical pyrometer. The STM topographic images were acquired *in situ*, while the dI/dV curves were acquired *ex situ* in a low temperature STM system.

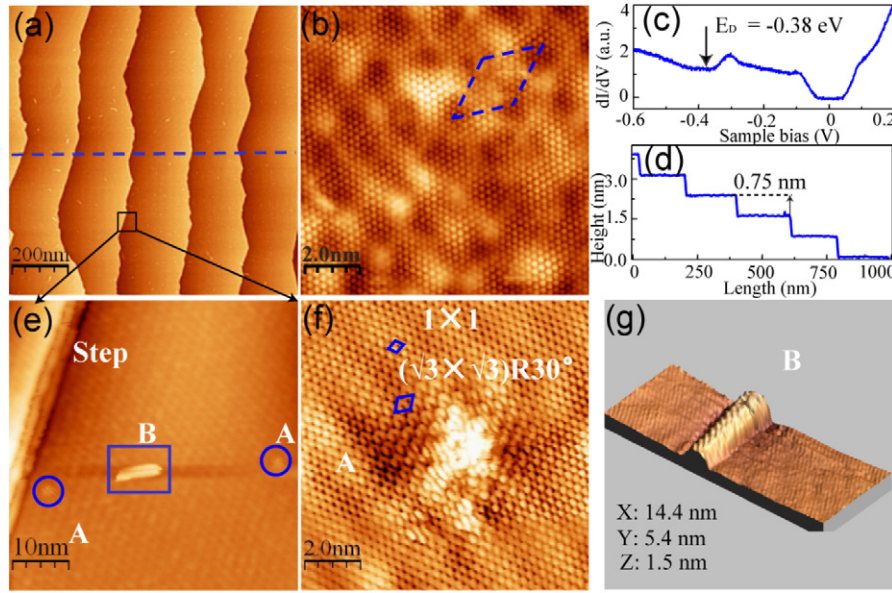


Figure 1. The surface morphology images and dI/dV curve of uniform bilayer graphene. The blue dashed diamond in (b) indicates the 6×6 unit cell of the interface layer. The dI/dV curve (c), showing the Dirac point located at 0.38 eV below the Fermi energy, was acquired at 2.2 K. (d) The line profile along the dashed line in (a). (e) The zoom-in image shows the step structure and two types of defects, i.e. A and B. (f) An atomically resolved STM image of type A defect. (g) A three-dimensional STM image of type B defect.

Figure 1(a) shows a typical STM image of the SiC surface after 80 cycles of flash annealing with a heating rate of $10 \text{ }^\circ\text{C s}^{-1}$, i.e. heating the SiC substrate from 650 to 1300 $^\circ\text{C}$ in 65 s. The surface is covered by uniform graphene layers consisting of regular ~ 200 nm wide terraces separated by 0.75 nm high steps. We use both the atomically resolved topographic image (figure 1(b)) and differential tunneling conductance (dI/dV) spectrum (figure 1(c)) to identify its thickness. In figure 1(b), the two distinct features, a triangular structure with a lattice constant of $\sim 0.24 \pm 0.02$ nm due to the Bernal stacking of graphene layers and a hexagonal reconstruction pattern attributed to the carbon-rich 6×6 reconstruction at the interface, are observed. The observations indicate that the uniform graphene is bilayer [9]. This is confirmed by the dI/dV spectrum measured on the terrace, where a gap of ~ 130 meV at the Fermi energy is observed. This is consistent with the previous results on bilayer graphene [10, 11]. Figures 1(d)–(g) show the details of the morphology of the uniform bilayer graphene. All the steps have the same height ~ 0.75 nm (figure 1(d)) and consist of triple SiC bilayer steps (figure 1(e)). There are mainly two types of defects (marked as A and B) on the terraces. Type A is a kind of atomic defect enclosed by the $\sqrt{3} \times \sqrt{3}$ pattern due to intervalley scattering of graphene (figure 1(f)) [12]. Type B is shown as a tubular mound, which does not perturb the atomic structure of the bilayer graphene (figure 1(g)), suggesting that it might be generated by strain due to the slight mismatched lattice constants and/or different thermal expansion coefficients between graphene and the SiC substrate [13, 14]. Based on a number of STM images, the defect density is estimated to be ~ 20 per $100 \times 100 \text{ nm}^2$.

To figure out the formation mechanism and to further reduce the defect density of the bilayer graphene, we studied

the morphology evolution under various annealing cycles (figures 2(a) and (b)) and heating rates (figures 2(c) and (d)). Figures 2(a) and (b) show the surface morphology during the intermediate graphitization process. After two cycles of flash annealing (figure 2(a)), the surface is irregularly covered by interfacial ($6\sqrt{3} \times 6\sqrt{3}$) (denoted ‘ $6\sqrt{3}$ ’ hereafter) layer (I) and monolayer graphene (M), as confirmed by atomically resolved images (inset in figure 2(a)). This is also confirmed by the result that step height is either one to three times 0.25 or 0.20 nm. The step of 0.25 nm corresponds to a SiC bilayer step and 0.2 nm the step between the $6\sqrt{3}$ layer and monolayer graphene [15], while steps of 0.5 and 0.75 nm are induced by the SiC bilayer step merging. After 20 cycles of flash annealing (figure 2(b)), the surface is covered by monolayer graphene (M) and bilayer graphene (B), the latter growing away from the SiC step edges with a finger-like structure. All the step heights, 0.4 , 0.75 and 1.1 nm, can be explained in terms of a bilayer SiC step (0.25 nm) and a graphene step (0.33 nm) [5]. After 80 cycles of flash annealing (figure 1), the surface is covered by uniform bilayer graphene with regular terraces separated by triple SiC bilayer steps. Although the surface morphology undergoes a remarkable change with increasing annealing, the terrace width is maintained at ~ 200 nm, which will be discussed later. In comparison, a faster heating rate ($60 \text{ }^\circ\text{C s}^{-1}$) leads to a similar uniform bilayer graphene with straighter steps but a larger defect density of ~ 50 per $100 \times 100 \text{ nm}^2$ (figure 2(c)), while a lower rate ($5 \text{ }^\circ\text{C s}^{-1}$) leads to an inhomogeneous graphene with pits and messy steps of various heights but a lower defect density of ~ 7 per $100 \times 100 \text{ nm}^2$ (figure 2(d)).

One common feature of the uniform bilayer graphene is that the steps consist exclusively of three SiC bilayer steps. Hupalo *et al* had proposed a model and attributed these triple

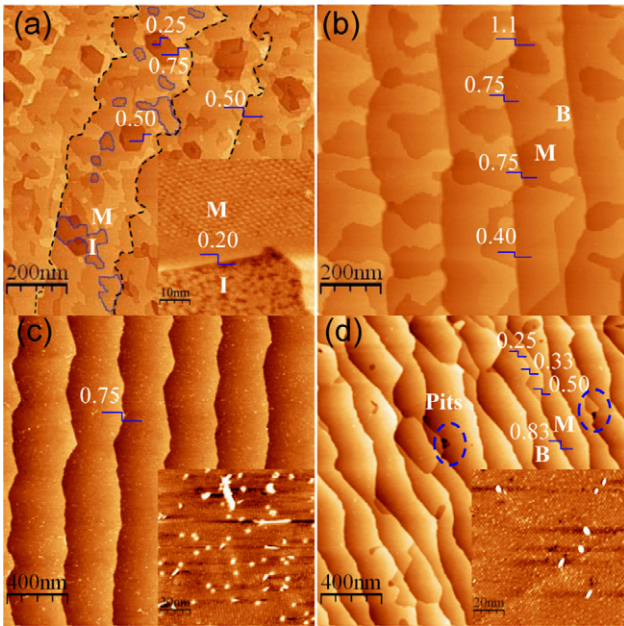


Figure 2. The surface morphology after being annealed at a heating rate of $10\text{ }^\circ\text{C s}^{-1}$ for various cycles: (a) two cycles, (b) 20 cycles. The dashed curves in (a) indicate the bunched step edges of 0.5 nm high and the areas enclosed by the blue lines correspond to the interfacial $6\sqrt{3}$ layer. The morphology after being annealed for 80 cycles at various annealing rate: (c) $60\text{ }^\circ\text{C s}^{-1}$, (d) $5\text{ }^\circ\text{C s}^{-1}$. The insets show the corresponding defect densities. The numbers demonstrate the step heights in units of nanometer.

SiC bilayer steps to the merging of three adjacent SiC single bilayer steps with different retracting speeds [5]. In the case of annealing at $1200\text{ }^\circ\text{C}$, the merging process may happen too fast to be identified experimentally [5]. We performed

cycles of flash annealing under Si flux at a lower temperature of $850\text{ }^\circ\text{C}$ for 2 min. Here, the surface is terminated with a Si-enriched 3×3 surface [16]. The morphology evolution and the corresponding line profiles with various annealing cycles are displayed in figures 3(a)–(c) and figures 3(d)–(f), respectively. After five cycles of annealing, the three adjacent terraces marked as 1, 2 and 3, separated by single bilayer steps, show different widths. After another 15 cycles of annealing, the two SiC terraces marked as 1 and 2 merge together to form a terrace marked as 12 with both step height and terrace width doubled. After a total of 45 cycles of annealing, the three adjacent terraces eventually merge to form a terrace marked as 123 with triple terrace width ($\sim 200\text{ nm}$) separated by triple bilayer steps (0.75 nm). These results clearly show that the three adjacent SiC bilayer steps retract at different speeds. Consequently, a bilayer step catches up with the other slowly retracting bilayer step to form a double bilayer step. When it catches up with the slowest moving step, a triple bilayer step is formed. This holds true for the graphitization process during flash annealing to $1300\text{ }^\circ\text{C}$, where the steps consist exclusively of three SiC bilayer steps and the terrace width is maintained at $\sim 200\text{ nm}$ (figures 1 and 2). It is worth noting that the step edges of the triple bilayer steps are quite straight.

Previous studies indicated that the $6\sqrt{3}$ interfacial layer plays a critical role in the growth kinetics. At the beginning of the graphitization process, SiC decomposition occurs both on terraces and at step edges. The domains of the interfacial layer may pin decomposing SiC steps, leading to pit formation [17]. On the other hand, once the $6\sqrt{3}$ interfacial layer forms, Si atoms have to either diffuse laterally to the step edges to desorb from there, or vertically pass through the $6\sqrt{3}$ interfacial layer to desorb from the surface. For the UHV

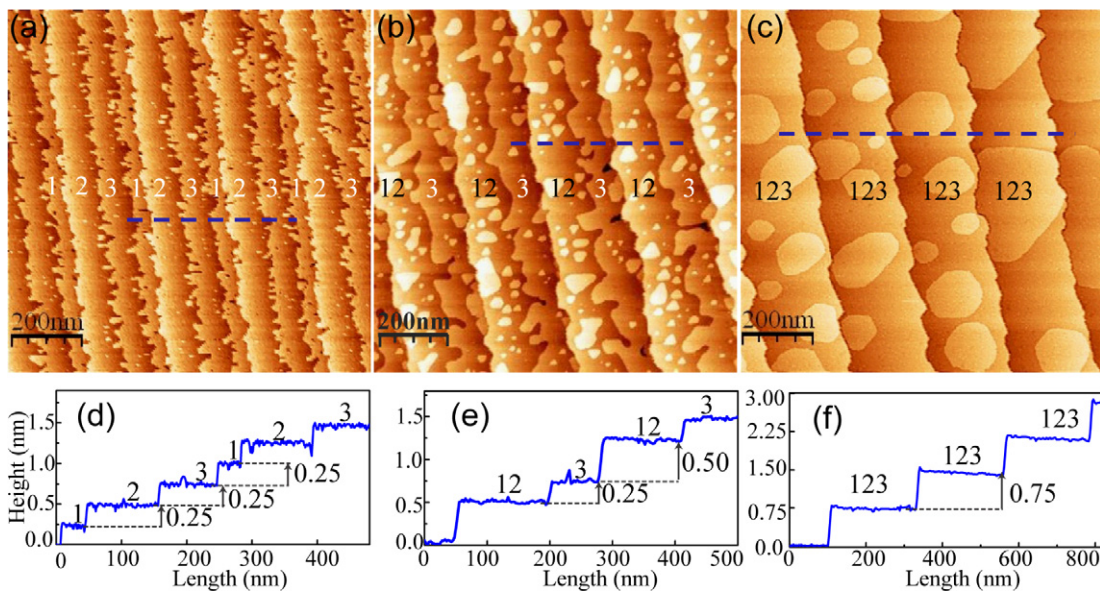


Figure 3. The morphology evolution and the corresponding line profiles after being annealed at $850\text{ }^\circ\text{C}$ under Si flux: (a) and (d) five cycles, (b) and (e) 20 cycles, (c) and (f) 45 cycles. The step height indicated by the arrow line is marked in units of nm. Some Si islands appear on the terrace due to excessive Si flux.

annealing, the lateral diffusion of Si atoms is energetically favorable and the SiC surface decomposes exclusively at steps [7]. Once a pit forms, its edges act as steps so that the decomposition there is promoted, which in turn causes the pits to further deepen. Hence, suppression of pit formation is one of the key factors for uniform thickness. As shown in figures 1 and 2, the annealing rate is the controlling parameter in determining the morphology of graphene in terms of step structure and defect density. During rapid heating to high temperature, the nucleation density of the interfacial layer is high, which leads to closely spaced domains and low tendency to form pits in turn [17]. Moreover, the rapid annealing suppresses the nonuniform decomposition rates of three adjacent SiC bilayer steps, leading to a uniform step structure with almost straight step edges (figure 2(c)). When the annealing rate is further lowered, pits form and pin the motion of SiC bilayer steps. Consequently, this leads to an irregular step structure (figure 2(d)) [17]. Meanwhile, annealing rate also affects the diffusion of the decomposed Si/C atoms and the strain relaxation of graphene layers. With a faster annealing rate, the released Si and C atoms have less time to diffuse through the overgrown graphene layers and at the graphene/SiC interface, respectively, and the strain in the graphene layers, due to the different thermal expansion coefficients of graphene and SiC substrate [14], is larger, which together leads to a higher density of defects on the surface.

Besides the above discussion, we point out that the interfacial layer, monolayer and bilayer graphene can together cover the surface at some stage of the growth due to the high annealing temperature of 1300 °C. Once monolayer graphene covers the entire surface, it acts as a barrier so that the graphitization process slows down [6]. The subsequent growth of bilayer graphene follows the step-flow growth mode with finger-like structure. Comparing with the standard usual long time UHV annealing, the rapid flash annealing to high temperature, similar to the conventional flash annealing used in Si [18], results in uniform desorption of Si atoms, high nucleation density of carbon atoms and uniform SiC decomposition rate at each SiC bilayer step, which eventually results in uniform bilayer graphene with regular step structure.

In conclusion, we have prepared large-scale uniform bilayer graphene by UHV flash annealing of a nominally flat Si-polar 6H-SiC(0001) substrate. The annealing rate, which is directly related to the nucleation of carbon atoms, the diffusion and desorption of Si atoms and strain relaxation, is the key factor to determine the step structure and defects

on graphene layers. To prepare uniform graphene layers by UHV annealing, rapid flash annealing is required. We expect that uniform monolayer graphene could be prepared by similar flash annealing of SiC at lower temperature with delicately controlled annealing rate. We would point out that the large-scale uniform graphene layers with regular step structure can be an ideal substrate for van der Waals epitaxy of the Fe-based superconductors and topological insulators.

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